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Claims

[c1] A DRAM device comprising:
a deep trench capacitor formed in a semiconductor substrate;
a storage cell including a vertical pass transistor having source and drain regions formed in a p- well, said drain region formed by a diffusion in said p- well outside said deep trench capacitor adjacent said first buried strap to conduct voltage to said trench capacitor; and
a control cell for controlling the threshold voltage of the vertical pass transistor according to a voltage of a gate connecting a second buried strap and diffusion region formed in the p-well region.

[c2] The DRAM device according to Claim 1, wherein a voltage of a gate connecting a second buried strap and diffusion region further controls the conductive state of the vertical pass transistor, said gate voltage comprising a wordline (WL) voltage controlling access to data stored in said deep trench capacitor via said vertical pass transistor.

[c3] The DRAM device according to Claim 2, wherein the second buried strap region and diffusion region formed in

said p- well region of said control cell is at a lower depth than the first buried strap region and diffusion region formed in said p- well region of said storage cell, whereby said threshold voltage of the vertical pass transistor is controlled in accordance with a depletion region formed by application of said WL voltage at said second buried strap region and diffusion region in the p- well region.

[c4] The DRAM device according to Claim 3, wherein said depletion region formed at said second buried strap and diffusion region pinches off the p-well to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower threshold voltage for turning on said vertical pass transistor during WL active state.

[c5] The DRAM device according to Claim 3, wherein said depletion region formed at said second buried strap and diffusion region does not pinch off the p-well at WL inactive state.

[c6] The DRAM device according to Claim 1, wherein a bitline voltage to be stored in said DRAM cell in a write operation is connected with a source of said vertical pass transistor.

[c7] The DRAM device according to Claim 1, wherein said drain of said vertical pass transistor is formed by a diffusion at said first buried strap.

[c8] The DRAM device according to Claim 1, wherein a gate at storage cell and control cell share the same wordline, the threshold voltage of the storage cell being modified according to the voltage at said wordline.

[c9] A method of fabricating a DRAM cell comprising the steps of:
a) forming a deep trench capacitor within a semiconductor substrate, said deep trench being filled with polysilicon and including a first buried strap layer and including a trench top oxide layer above the first buried strap;
b) forming a vertical pass transistor including a gate conductor, a gate oxide and a drain region formed in a p- well by a diffusion in said p- well region outside said deep trench adjacent said first buried strap for conducting voltage to said deep trench capacitor;
c) forming a control cell for controlling the threshold voltage of the vertical pass transistor according to a voltage at a gate connecting a second buried strap and diffusion region formed in the p-well region.

[c10] The method according to Claim 9, wherein a voltage of a gate connecting said second buried strap and diffusion

region further controls a gate threshold voltage of the vertical pass transistor, said gate voltage comprising a wordline (WL) voltage controlling access to data stored in said deep trench capacitor via said vertical pass transistor.

[c11] The method according to Claim 10, wherein said gate formed at said storage cell and control cell share a same wordline, the threshold voltage of the storage cell being modified according to the voltage at said wordline.

[c12] The method according to Claim 9, wherein the step c) of forming a control cell including a second buried strap and diffusion region formed in the p-well region, comprises forming said second buried strap region and diffusion region formed in said p- well region of said control cell at a lower depth than the first buried strap region and diffusion region formed in said p- well region of said storage cell, whereby said threshold voltage of the vertical pass transistor is controlled in accordance with a depletion region formed by application of said WL voltage at said second buried strap region and diffusion region in the p- well region.

[c13] The method according to Claim 12, wherein said depletion region formed at said second buried strap and diffusion region extends sufficiently into the p-well to ef-

fectively pinch off the p-well to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower threshold voltage for turning on said vertical pass transistor during WL active state.

[c14] The method according to Claim 12, wherein said depletion region formed at said second buried strap and diffusion region does not extend sufficiently into the p-well and thus does not effectively pinch off the p-well to disconnect the p-well pinch off the p-well at WL inactive state.

[c15] A method of improving performance of a DRAM cell comprising:

a) providing two deep trenches, one trench including a vertical storage cell and deep trench capacitor for storing data and a second trench including a vertical control cell for controlling voltage at a p-well region separating the vertical storage and control cells;

b) applying a voltage to a common conductor connecting a gate of each said vertical storage and control cell, said voltage being of a value enabling pinch-off of said p-well structure to thereby render said p-well region into a p-well floating condition having a first floating region and a second conductive region, wherein said p-well floating condition decreases the threshold voltage of

said vertical storage cell when in an on-state as compared to when in an off-state thus resulting in increased gate over-drive and drive current.

[c16] The method as claimed in Claim 15, wherein said common conductor is a wordline having a wordline active or inactive voltage state, said step b) of applying a voltage to a common conductor including: applying a wordline active voltage to enable reduction of storage cell gate threshold voltage to thereby increase drive current, or applying a wordline inactive voltage to turn off said storage cell, said wordline voltages being simultaneously applied to both gates of the storage and control cells.

[c17] The method as claimed in Claim 15, wherein a vertical storage cell for storing data includes a vertical pass transistor having a drain diffusion region formed in the p-well at a first buried strap location connecting said trench capacitor and, said vertical control cell includes a second diffusion region formed in the p-well at a second buried strap location for controlling conductive state of said vertical pass transistor.

[c18] The method as claimed in Claim 17, wherein said second diffusion region formed in the p-well at a second buried strap location is lower in depth than the drain diffusion region formed in the p-well at a first buried strap loca-

tion.

[c19] A vertical transistor device comprising:
two trenches, each trench including a gate element for the device, a first buried strap forming a corresponding drain or source diffusion region for the device and each located at equal depths within said trenches, and, a second buried strap forming corresponding control diffusions formed in a p- well region separating said two trenches, each second buried strap located at equal depths within said trenches below corresponding first buried straps and electrically connected to said gate for receiving applied voltage thereat,
whereby a voltage threshold of the vertical transistor device is controlled in accordance with depletion regions formed in the p-well at corresponding control diffusions at each said second buried strap in response to application of a gate voltage at each trench.

[c20] The vertical transistor device as claimed in Claim 19, wherein the formed depletion regions extend sufficiently into the p-well to effectively merge and pinch off the p-well region to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower voltage threshold for turning on the vertical transistor device.